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THOMPSON & KNIGHT

L.L.P.
ATTORNEYS AND COUNSELORS
1700 PACIFIC AVENUE
SUITE 3300
DALLAS, TEXAS 75201
(214) 969-1700
IP FAX (214) 999-9024AUSTIN
(512) 469-6100 / FAX (512) 469-6180

DIRECT DIAL: (214) 969-1290

FACSIMILE COVER LETTERPlease wait for Reply confirmation

TO: The United States Patent and Trademark Office

FROM: Yanela Carpenter - 214-969-1376

SUBJECT: U.S. Patent No.: 6,948,098
Serial No.: 09/822,052FILE: 021615.500038
CIRCUITS AND METHODS FOR DEBUGGING AN
EMBEDDED PROCESSOR AND SYSTEMS USING THE SAMEDATE: June ¹⁶ 11, 2008

FAX NO.: (571) 273-8300

Certificate

JUN 18 2008

of Correction

ATTENTION CERTIFICATE OF CORRECTIONS BRANCH

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555555 099862 DALLAS 2038967.1

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NO. 8786 P. 2

THOMPSON & KNIGHT LLP

ATTORNEYS AND COUNSELORS

1700 PACIFIC AVENUE • SUITE 3300
DALLAS, TEXAS 75201-4693(214) 969-1700
FAX (214) 969-1751
www.tklaw.comDirect Dial: (214) 969-1749
E-mail: james.murphy@tklaw.com

June 12, 2008

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Attn: Certificate of Corrections Branch
P. O. Box 1450
Alexandria, Virginia 22313-1450**RECEIVED**
CENTRAL FAX CENTER**JUN 16 2008**

Re: U. S. Patent No. 6,948,098 B2
Issued: September 20, 2005
Title: CIRCUITS AND METHODS FOR DEBUGGING AN
EMBEDDED PROCESSOR AND SYSTEMS USING
THE SAME
Our File: 021615.500038

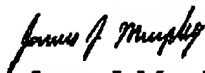
Dear Sirs:

Please be advised that a Request for a Certificate of Correction for the above-referenced patent was filed with the United States Patent and Trademark Office on January 10, 2006. Enclosed is a copy of this Request for your convenience. We received a postcard from the USPTO dated January 30, 2006, confirming that a Request for a Certificate of Correction was received for the above-referenced patent, copy of this postcard is also enclosed for your convenience.

On February 7, 2007, we filed a Status Inquiry, I am enclosing a copy of the Auto-Reply Facsimile Transmission issued by the USPTO. Please be advised that to date, we have not received a certificate of correction for this patent nor anything further from the USPTO regarding this matter.

Applicant respectfully requests a status update of the Request for a Certificate of Correction filed on January 10, 2006.

Very truly yours,



James J. Murphy

JJM/yoc
Enclosure

021615 500038 DALLAS 2359828.1

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JUN. 16. 2008 3:26PM THOMPSON KNIGHT 30:40 AM PAGE 1/001 NO. 8786 P. 3
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TO: Fax Sender at 214 969 1751
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| <u>FACSIMILE COVER LETTER</u> | | | |
| TO: | The United States Patent and Trademark Office | | PHONE NO.: |
| FROM: | James J. Murphy | | |
| SUBJECT: | U. S. App. No. 09/133,052 TITLE: CIRCUITS AND METHODS FOR DEBUGGING AN EMBEDDED PROCESSOR AND SYSTEMS USING THE SAME | | |
| CLIENT/FILE # | 021615-500038 | | |
| Date: | February 7, 2007 | | |
| PHONE EXT.: | 1378 | | |
| FAX NO.: | (571) 273-8300 | | |
| NO. OF PAGES: 6 | | | |
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| PAGE 15 * RCVD AT 2/8/2007 11:20:41 AM [Eastern Standard Time] * SVR:USPTO-EFXXF-15 * DNIS:2738300 * CSID:214 969 1751 * DURATION (mm:ss):22:42 | | | |

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THOMPSON & KNIGHT LLP

ATTORNEYS AND COUNSELORS

1700 PACIFIC AVENUE • SUITE 3300
DALLAS, TEXAS 75201-4693(214) 989-1700
FAX (214) 989-1751
www.tklaw.comDirect Dial: (214) 969-1749
E-mail: james.murphy@tklaw.com

February 7, 2007

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CENTRAL FAX CENTER****JUN 16 2008**Commissioner for Patents
Attn: Certificate of Corrections Branch
P. O. Box 1450
Alexandria, Virginia 22313-1450**Re: U. S. Patent No. 6,948,098 B2
Issued: September 20, 2005
Title: CIRCUITS AND METHODS FOR DEBUGGING AN
EMBEDDED PROCESSOR AND SYSTEMS USING
THE SAME
Our File: 021615.500038**

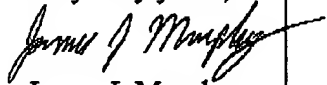
Dear Sirs:

Please be advised that a Request for a Certificate of Correction for the above-referenced patent was filed with the United States Patent and Trademark Office on January 10, 2006. Enclosed is a copy of this Request for your convenience.

Please be advised that to date, we have not received a certificate of correction for this patent nor anything further from the USPTO regarding this matter.

Applicant respectfully requests a status update on the certificate of correction for this patent.

Very truly yours,


James J. Murphy

Enclosure

021615 500038 DALLAS 2142467.1

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JAN 30 2006

A request for a Certificate of Correction has
been received for U.S. Patent 6948098

Thompson & Knight LLP.

JAMES J. MURPHY
THOMPSON + KNIGHT LLP
1700 PACIFIC AVE., STE
DALLAS, TX 75201-4693

JAN 30 2006

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PTO/SB444 (04-05)

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UNITED STATES PATENT AND TRADEMARK OFFICE CERTIFICATE OF CORRECTION

Page 1 of 3

PATENT NO. : 6,948,098 B2

APPLICATION NO.: 09/822,052

ISSUE DATE : September 20, 2005

INVENTOR(S) : Sanjay Ramakrishna Pillay and Raghunath Kirisha Rao

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 19, Line 67, last paragraph, "he" should be -- the --;

Column 20, Line 2, "706k" should be -- 706 --;

Column 25, Line 42, "disturbe" should be -- disturb --;

Column 25, Line 46, "688" should be -- 68 --;

Column 27, Line 2, "FIFO_1 STATE" should be -- FIFO_1_STATE --;

Column 27, last line, "microprocessor" should be -- Microprocessor --;

Column 40, Line 17, "STC_COUNTER0" should be -- STC_COUNTER0 --;

Column 42, last line, after "weak1", the following sentence should be inserted:
-- Tables 173-175 illustrate the mapping for the microprocessor 101 memory access projection registers. --;

Column 48, Table 1, description for LineLength, line beginning "dots = 1", "andld" should be
-- andld --;

MAILING ADDRESS OF SENDER (Please do not use customer number below):

James J. Murphy, Thompson & Knight LLP
1700 Pacific Avenue, Suite 3300
Dallas, Texas 7529104693

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PATENT NO. : 6,948,098 B2

APPLICATION NO.: 09/822,052

ISSUE DATE : September 20, 2005

INVENTOR(S) : Sanjay Ramakrishna Pillay and Raghunath Kirisha Rao

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 57, Table 26, Line 6 of header, "master" should be -- masters --;

Column 57, Table 27, Line 4 of header, "master" should be -- masters --;

Column 58, Table 28, Line 5 of header, "master" should be -- masters --;

Column 60, Table 34, Type for "SDEC" should be -- R/W --;

Column 64, Table 49, Lines 30, 33, 36 and 39, "harware" should be -- hardware --;

Column 75, Table 65, Line 24, should read -- prevents engine from starting if it has --;

Column 88, Table 95, Line 1 of table, "d_Manufacturer" should be -- d_iManufacturer --;

Column 95, Table 111, First line of Header should read -- EP2DESC1 (Endpoint 2 Descriptor1, --;

Column 97, Table 113, the Reset Value for "ep3_wMaxPacket Size" should be -- 0x40 --;

Column 102, Table 130, Line 61, "s_pmdk" should be -- sp_mdk --;

Column 109, Table 146, Line 1 of header should begin with -- GPIO Interrupt Mask Register --;

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Page 3 of 3

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APPLICATION NO.: 09/822,052

ISSUE DATE : September 20, 2005

INVENTOR(S) : Sanjay Ramakrishna Pillay and Raghunath Kirisha Rao

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 109, Table 147, next to last line of table, "generated" should be -- generates --;

Column 111, Table 148, Line 12, "GPIO[2]" should read -- GPIO[12] --;

Column 116, Table 157, second line of table "sae" should be -- case --;

Column 125, Table 177, Function Block for line beginning "8008_0000 - 8008_FFFF" should read
-- Remap Pause Control --;

Column 129, Table 179, Function Block for line beginning "8003 0000 - 8003 FFFF" should read
-- Battery Volume Checker --;

Column 129, Table 180, second line of header, "Defirdtton" should be -- Definition --

Spanning Columns 131 & 132, Table 188, the description for DiePad 12 should read
-- DCL2/GPIO1 pin <12> default) --;

Spanning Columns 131 & 132, Table 188, the Signal Name for 17 (second occurrence) should be
-- _VDD_CORE --.

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